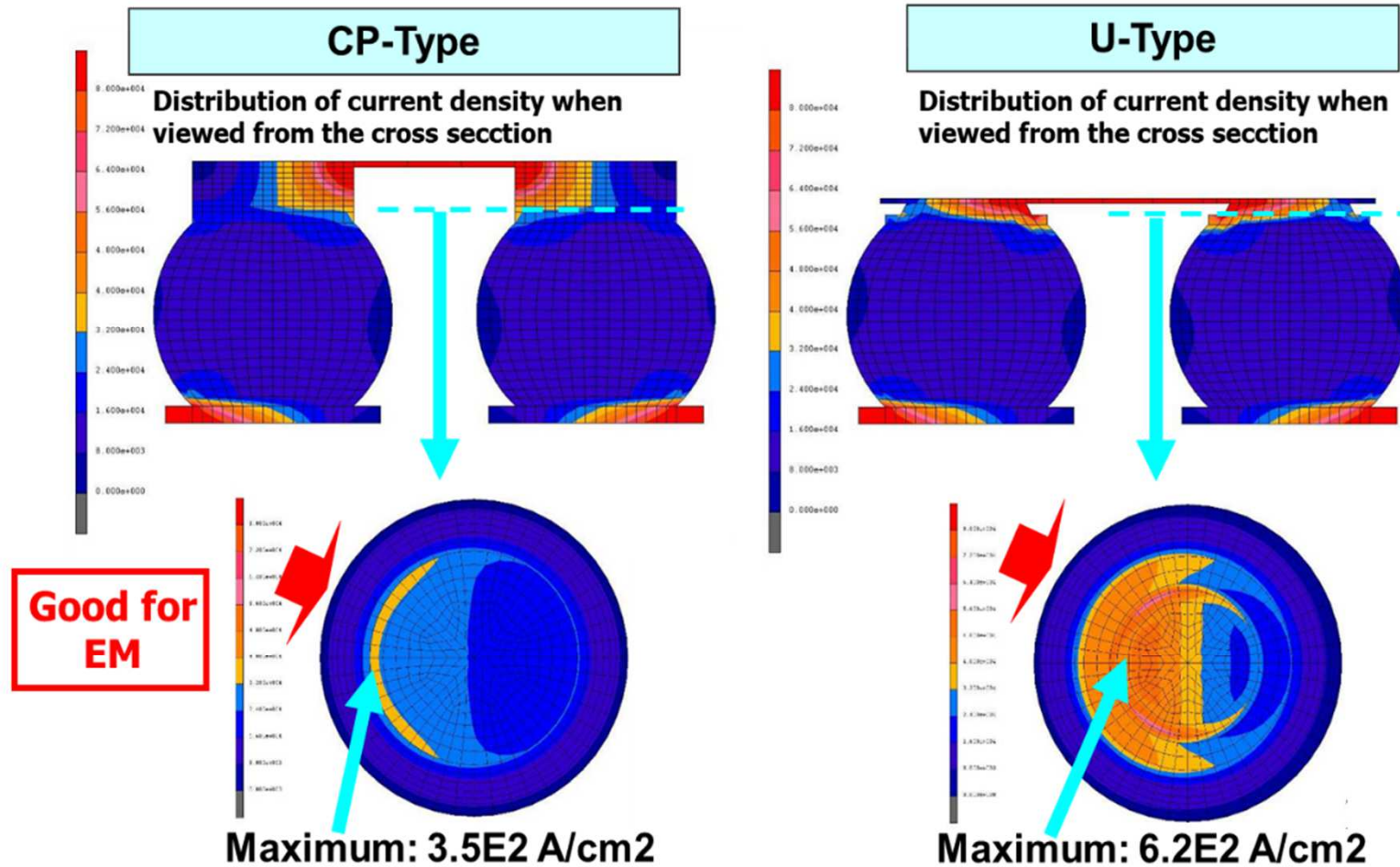


High Reliability WLP Technology

High Reliability WLP Technology

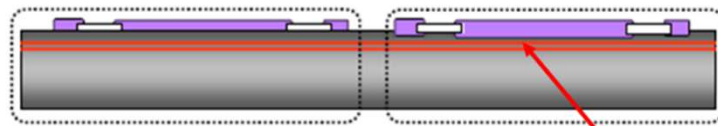
Current density simulation



Current density in the solder interface of CP-Type is 56% of U-Type

High Reliability WLP Technology

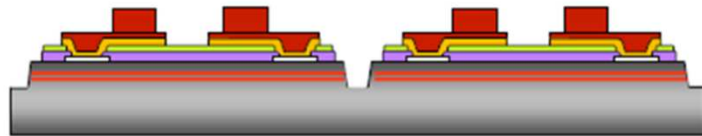
Cross-sectional view when Low-k layer is grooved



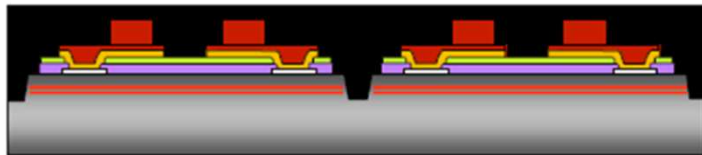
Incoming

 : 1 Chip

Low-k layer

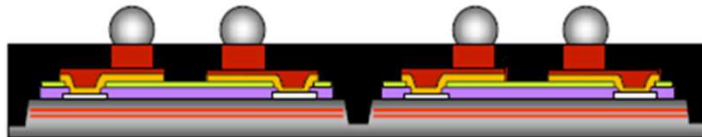


Laser grooving

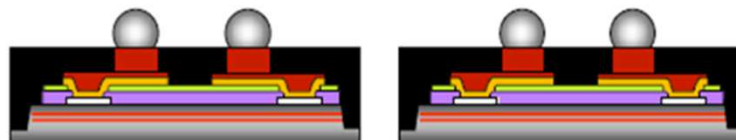


Encapsulation Resin

(The side of Low-K is also covered with resin and is highly reliable.)



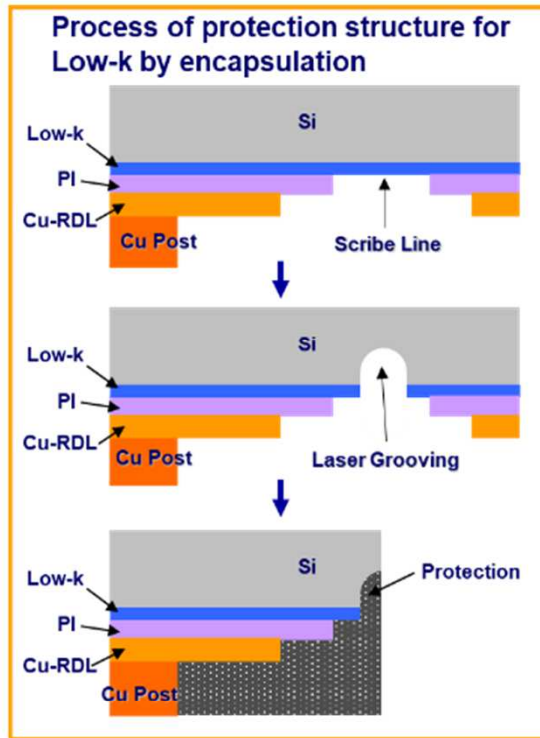
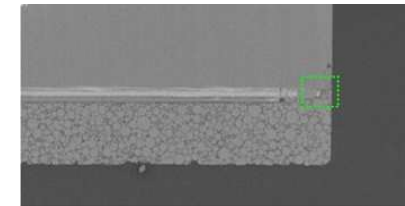
Solder Ball Attach



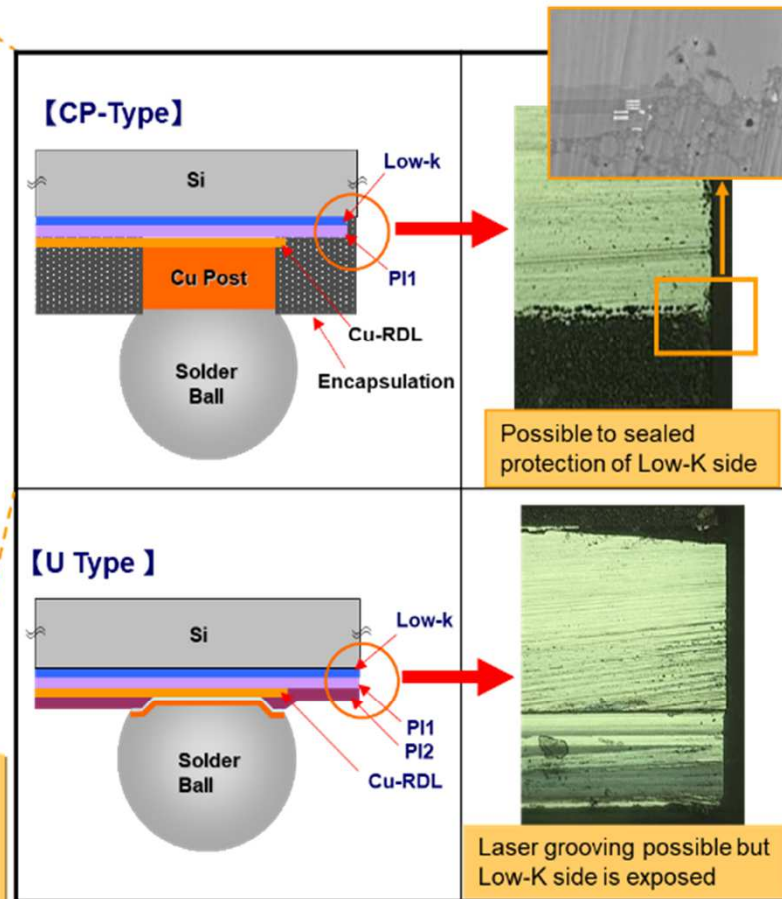
Dicing

High Reliability WLP Technology

Cross-sectional view when Low-k layer is grooved



CP-Type is prevent peeling of the Low-k layer by sealing the side walls of fragile Low-k layer by encapsulation.



High Reliability WLP Technology

Reliability results

Test Items	Test condition	N	Test timing	Result	Judgment
				Lot 1	
Reflow	85°C/85% 168hr⇒ >255°C 30sec. 10X (JEDEC J-STD-020D Moisture Level1)	45	Initial	0/45	Pass
			After reflow	0/45	
PCT	Pre-condition ⇒ 121°C 100% 168hr	50	Initial	0/50	Pass
			168hr	0/50	
HTS	Pre-condition ⇒ 150°C、500hr、1000hr	50	Initial	0/50	Pass
			500hr	0/50	
			1000hr	0/50	
TCT	Pre-condition ⇒ -65°C~150°C、500cycle、1000cycle	50	Initial	0/50	Pass
			500cycle	0/50	
			1000cycle	0/50	
THB	Pre-condition ⇒ 85°C 85%RH、3.5V 168hr,500hr,1000hr	22	Initial	0/22	Pass
			168hr	0/22	
			500hr	0/22	
			1000hr	0/22	

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Thank you very much for your understanding in advance.